Ac-dc Difference at Cryogenic Temperatures

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Abstract: *We are continuing the development of a new primary standard for ac-dc difference that utilizes a superconducting resistive transition-edge device as the sensor. The most recent improvements to the Cryogenic Thermal Transfer Standard (CTTS) include on-chip magnetic shielding which has reduced the coupling of magnetic fields from the heaters into the transition-edge sensor; however, measurements indicate that errors still persist in the CTTS. To isolate these errors, we propose an experiment to measure two CTTS chips inside the cryostat, where transmission line and similar effects will be negligible. In addition, we are redesigning the sensor chip to improve its performance at higher power levels.*

Introduction and Present Status

The most accurate RMS measurements of voltage and current are made by comparing the heating effect of an unknown ac signal to that of a known dc signal using a thermal converter. Thermal converters are usually composed of one or more thermocouples arranged along a heater structure, generally a wire or thin-film conductor. The most accurate thermal converters are multijunction thermal converters [1], which are used at most national metrology institutes as the basis for ac voltage and current calibrations. The limiting factors for the accuracy of these thermal converters at low voltages and audio frequencies are, to a great extent, thermal and thermoelectric effects that are temperature dependent. We are developing a thermal transfer standard that operates at temperatures below 10 K, where these thermal effects are expected to be quite small. The Cryogenic Thermal Transfer Standard (CTTS) is especially suitable for use at extremely small input power levels, where an accurate primary standard does not as yet exist. We anticipate that this effort will eventually lead to the introduction of a new class of primary

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standard for ac-dc difference calibrations, with uncertainties an order of magnitude less than present primary standards.

The CTTS is based on a superconducting resistive transition-edge sensor (TES) chip fabricated from a niobium-tantalum (NbTa) alloy. In the normal operation of the CTTS, the temperature of the chip is brought to the transition temperature (T_c) of the TES by applying current to a trim resistor deposited adjacent to the TES on the silicon substrate. An unknown ac signal and both polarities of a known dc signal are then applied in a timed sequence to the signal heater. The changes in temperature of the chip between applications of the ac and dc quantities are reflected in variations of the resistance of the TES. The resistance of the TES is monitored using a resistance bridge, and the resistance of the TES is brought back to its original value by adjusting the current in the trim heater. By monitoring the value of the current required to match the unknown signal to the known dc signal, the ac-dc difference of the CTTS can be determined.

The original CTTS [2] was found to have large ac-dc differences at frequencies above 1 kHz, and the ac-dc difference also changed with signal level. The frequency dependence at high frequencies was partially addressed by replacing the original normal-metal input transmission line with a superconducting transmission line fabricated from a crystalline thin film of $YBa_2Cu_3O_x$ (YBCO) deposited on a substrate of lanthanum aluminate [3]. This transmission line extends from the nitrogen shield (maintained at 77 K) to the interior of the helium shield. Since the T_c of YBCO is about 90 K, the superconducting transmission line is well below its transition temperature, providing excellent thermal isolation to the experimental platform as well as better electrical properties than the original transmission line. Measurements of the CTTS using this transmission line indicate that the bulk of the high-frequency error has been resolved.

The dependence of ac-dc difference on input signal level is indicative of magnetic field suppression of the T_c of the NbTa. The magnetic field coupling from the signal and trim heaters with a dc signal applied is significantly different from the coupling with ac signals applied; consequently the T_c will differ in response to the type of signal applied. An attempt to overcome this effect by fabricating a new chip with larger spacing between the heaters and TES, and with superconducting niobium ground planes was generally successful [4]. Chip layouts of the original CTTS chip and the newer, shielded chip are shown in Figure 1, and the difference in magnetic field profiles in figure 2.

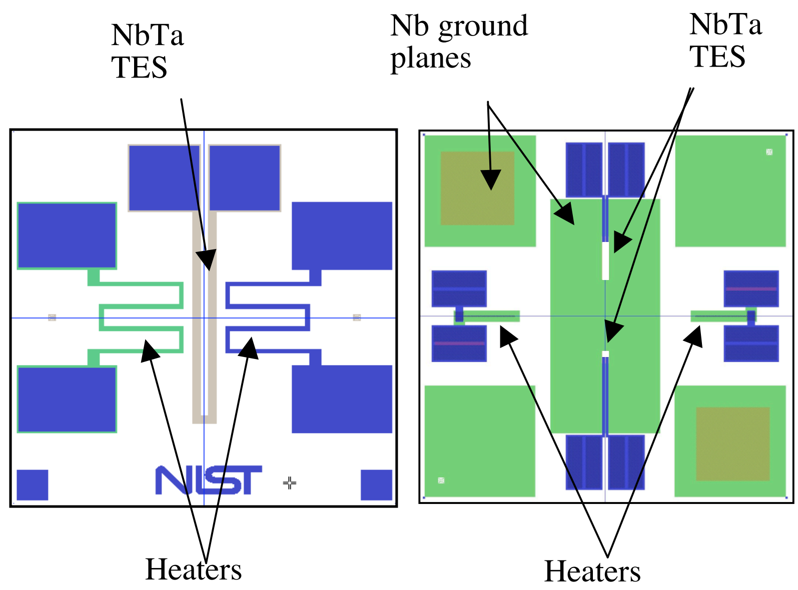

Figure 1. Chip layouts of the original TES chip (left) and the new chip (right).

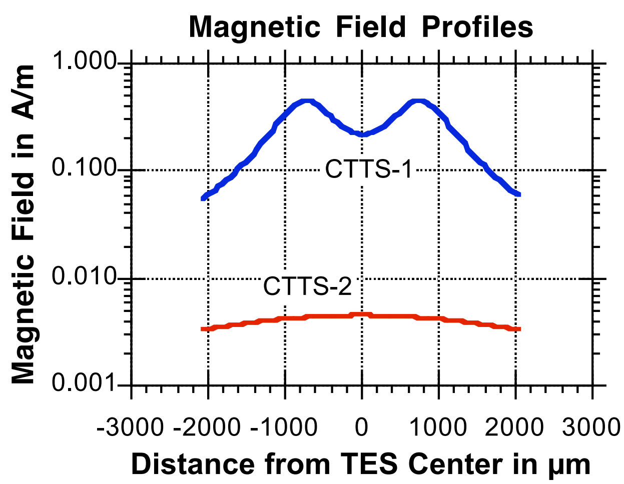

Figure 2. Calculated magnetic fields resulting from the heater currents for the original sensor chip (CTTS-1) and the new, shielded chip (CTTS-2), shown as a function of position on the TES chip. The fields present on the CTTS-2 chip are reduced still further by the superconducting shielding on the chip.

Future Work

Although significant progress has been made in improving the performance of the CTTS, significant sources of error persist. These sources of error are likely to include magnetic coupling amongst the niobium ribbons carrying the measurement signals from the experimental platform to the TES chip, errors in the measurement of the TES resistances, and residual errors in the input transmission structure. We are planning to address these problems as follows:

1) Owing to the design of the experimental platform, the ac and dc measurement signals, as well as the signals for the resistance measurements and feedback current, are routed through Nb ribbons from tracks on the platform base to the experimental chip, a distance of approximately 5 cm. These ribbons are unshielded, and it is likely that magnetic field coupling, which varies with signal level, frequency, and signal type (ac or dc) exists between the ribbons. We are addressing this problem by redesigning the experimental platform to separate the signal paths. We are also addressing the problem of wire bonding onto the TES chip by considering alternate methods of making contact with the pads on the chip.
2) The superconducting YBCO transmission line significantly improved the performance of the CTTS, particularly at frequencies above 1 kHz; however, the ac and dc signals are still carried from the platform base to the experimental platform by Nb ribbon wires. In addition to the redesign of the experimental platform, we propose an experiment to measure two TES chips against one another inside the cryostat. This will move the plane of reference for thermal voltage converter measurements from outside the cryostat (and about 25 cm from the CTTS chip) to a position adjacent to the two chips, eliminating any residual effects from the transmission line and input leads. In addition, the testing of the two thermal converters in a similar environment offers an opportunity to demonstrate the viability of the technology.
3) To evaluate the contributions to the ac-dc difference from the measurements of the TES resistance, we are investigating different resistance bridges. Changing the arrangements of the leads carrying the current and sense leads onto the experimental platform will also reduce the coupling between these leads, resulting in more stable resistance measurements.

A conceptual drawing of the platform planned for the two-converter measurement is shown in Figure 3. The drawing shows the additional platform required for mounting two TES chips, as well as a new transmission line structure to bring the signals on to the chip. The new platform is designed to mate with the existing platform, so that the present temperature-control scheme remains unchanged.

In addition to the twin-TES experiment, work is underway to fabricate a new TES chip with higher resistance heaters and the TES suspended on a thin dielectric membrane similar to that used in thin-film multijunction thermal converters [5]. This will enhance the isothermality of the temperature-sensing region of the chip, provide for better temperature control, and allow us to operate the CTTS at greater signal powers. In addition, problems with the measurements of the TES resistance will be addressed, possibly through technology being developed at NIST for Johnson Noise thermometry. The new design will also provide improved signal paths for the signal, feedback, and resistance leads.

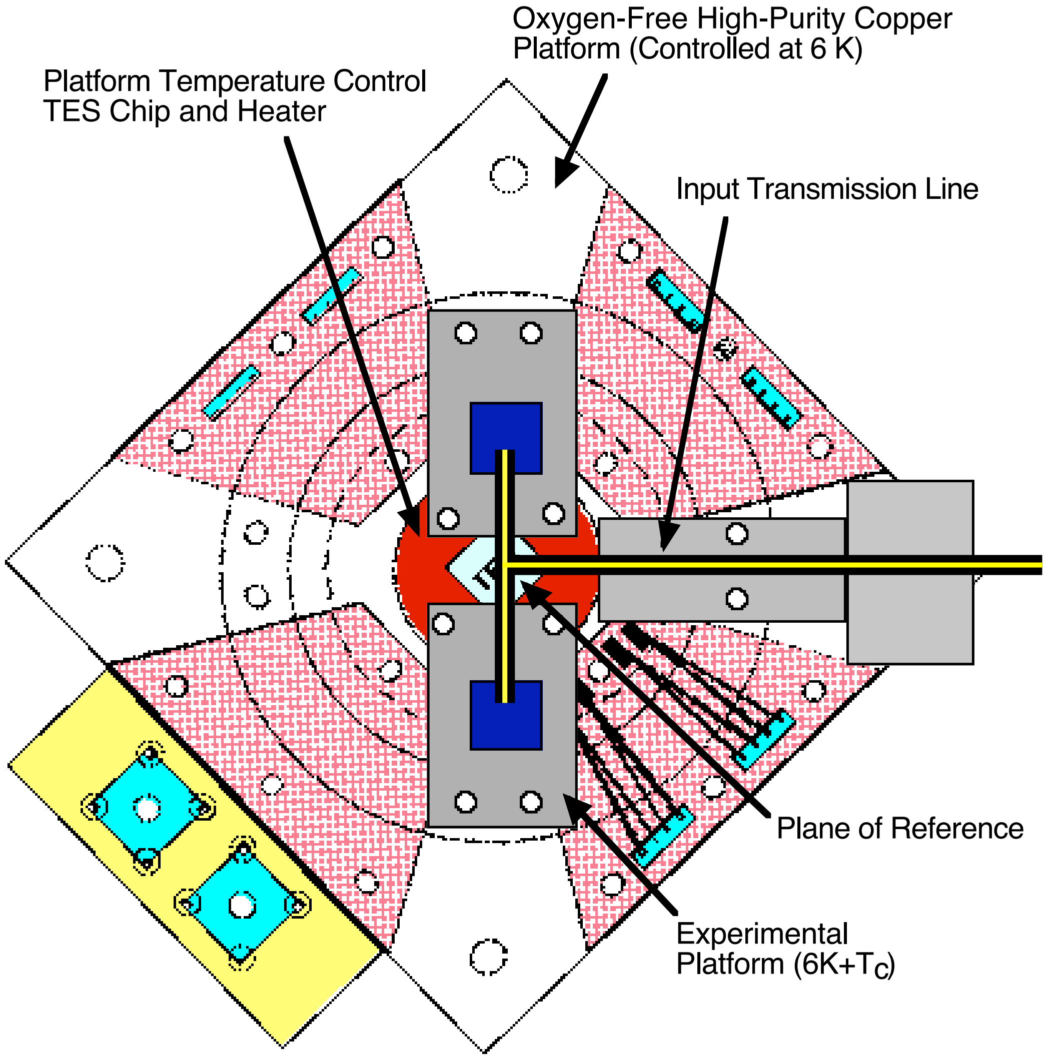

Figure 3. Proposed design for twin-TES experimental platform.

Conclusions

We are planning a new set of experiments on the CTTS to determine the promise of using superconducting technology to develop a new primary standard for ac-dc difference. The most immediate experiment involves rebuilding the experimental platform in order to measure two TES chips against each other *in situ*. This experiment removes any transmission line effects in the signal leads. The second, more ambitious experiment includes redesigning the TES chip to increase its efficiency, fabricating a new platform with improved signal path geometry, and improving the measurements of the TES resistance.

References

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